Single-Cycle-PLL Detection for Real-Time FM-AFM Applications

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***Abstract*—In this paper we present a novel architecture for phase-locked loop (PLL) based high-speed demodulation of frequency-modulated (FM) atomic force microscopy (AFM) signals. In our approach, we use single-sideband (SSB) frequency upconversion to translate the AFM signal from the position sensitive detector to a fixed intermediate frequency (IF) of 10 MHz. In this way, we fully benefit from the excellent noise performance of PLL-based FM demodulators still avoiding the intrinsic bandwidth limitation of such systems. In addition, the upconversion to a fixed IF renders the PLL demodulator independent of the cantilever's resonance frequency, allowing the system to work with a large range of cantilever frequencies. To investigate if the additional noise introduced by the SSB upconverter degrades the system noise figure we present a model of the AM-to-FM noise conversion in PLLs incorporating a phase-frequency detector. Using this model, we can predict an upper corner frequency for the demodulation bandwidth above which the converted noise from the single-sideband upconverter becomes the dominant noise source and therefore begins to deteriorate the overall system performance. The approach is validated by both electrical and AFM measurements obtained with a PCB-based prototype implementing the proposed demodulator architecture.**

***Index Terms*—Atomic force microscopy, frequency-modulated atomic force microscopy (FM-AFM), noise analysis, phase-locked loop (PLL), single-cycle detection.**

I. Introduction

OVER the past decade, with the advent of advances in cantilevers, instrumentation and control [1]–[4], high speed atomic force microscopy (AFM) has become a new frontier in nanocharacterization. As an important example, high speed AFM has gained significant attention in the field of life science as a tool for studying biological structures at the cellular and subcellular level [1], [5]–[11]. In contrast to conventional AFM applications in material science where imaging time is of minor importance, in biological AFM applications one is often interested in high temporal resolutions in order to study biological processes with relatively fast time scales [1], [6], [7], [11].

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In classical amplitude modulated (AM) AFM, the achievable scan rate is directly proportional to the 3-dB bandwidth of the utilized cantilever. Since this 3-dB bandwidth is proportional to the ratio of the cantilever's resonance frequency, f_{cant}, and its quality factor, Q, one frequent approach towards higher scan rates in AM-AFM makes use of cantilevers with increased resonance frequencies. However, these high-resonance-frequency cantilevers most of the time also display an increased stiffness, resulting in an enhanced quality factor and thereby rendering the overall increase in achievable scan rate in classical AM-AFM marginal.

In frequency modulated (FM) AFM this quality factor-bandwidth tradeoff does not exist because the cantilever can respond instantaneously, i.e., without bandwidth limitations, to perturbations in its oscillation frequency, cf. e.g. [12]–[14], and the theoretically achievable bandwidth in this operating mode is eventually only limited by the cantilever resonance frequency itself. Although most high-resolution FM-AFM experiments are conducted in vacuum, it has already been demonstrated that molecular resolution FM-AFM is possible also in liquids [15]. Therefore, in order to fully benefit from the large theoretically achievable bandwidth and resolution of FM-AFM, there is need for high-speed FM demodulators which can provide both the excellent noise performance required in high-resolution AFM applications and demodulate signals with modulation bandwidths as large as the cantilever resonance frequency, i.e., provide a true single-cycle detection. Here, the term true single-cycle detection refers to the fact that the detector can detect variations in the modulating signal within one period of the carrier frequency, i.e., with a modulation rate larger than one half of the carrier frequency.

To account for both of these contradicting design goals, we propose the use of a single-sideband (SSB) upconverter in combination with a subsequent phase-locked loop (PLL) based FM demodulator. Thanks to their closed-loop structure, PLL-based FM demodulators show the best noise performance of all available FM demodulator architectures, cf. [16]. However, their demodulation bandwidth is limited to a value between one fifth and one tenth of their input carrier frequency, cf. [16]. Therefore, a standalone PLL-based FM demodulator cannot be used when attempting to fully exploit the available signal bandwidth provided by the cantilever. To overcome this problem, we use an SSB upconverter which translates the center frequency of the AFM signal from the cantilever resonance frequency to an intermediate frequency (IF) of 10 MHz without introducing a frequency component at the so-called image frequency, i.e., the frequency of the undesired sideband, which could perturb the

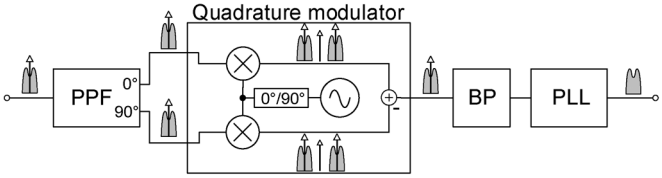

Fig. 1. Illustration of the proposed system architecture.

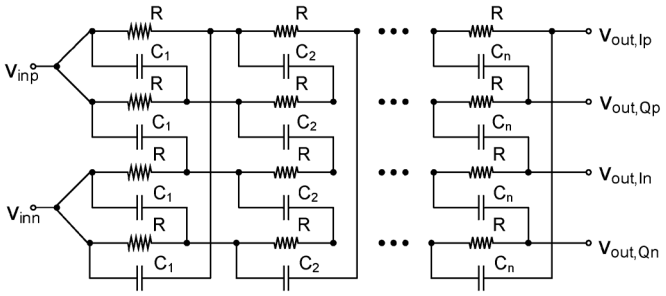

Fig. 2. Schematic of the passive polyphase filter generating the quadrature signals for the SSB modulator.

lock-in process of the subsequent PLL. In this way, we can select a PLL demodulation bandwidth up to 1 MHz, allowing to fully exploit the intrinsic bandwidth of cantilevers with resonance frequencies up to 1 MHz for high-speed, high-resolution FM-AFM.

The paper is organized as follows: In Section II, we present a detailed overview of the proposed FM demodulator architecture and its individual building blocks. Section III then deals with the problem of AM-to-FM noise conversion in the PLL's phase detector (PD). More specifically, we introduce an analytical model which allows the prediction of the maximally achievable demodulation bandwidth without SNR degradation due to the additional AM noise introduced by the SSB modulator. We then present the details of a PCB-based prototype of the proposed architecture in Section IV, which is used to perform the electrical performance characterization of Section V. In addition to the electrical characterization, in Section V we provide preliminary FM-AFM images as an in-situ proof-of-principle for the proposed approach. Finally, we conclude the paper with a short summary and a brief outlook on future work in Section VI.

II. System Overview

The architecture of the proposed highspeed FM demodulator is shown in Fig. 1. According to the figure, the AFM signal coming from the position sensitive detector is fed into a polyphase filter (PPF) which generates the quadrature baseband signals required for the subsequent SSB upconversion. The SSB modulator translates the center frequency of the AFM signal from the cantilever resonance frequency f_{cant} to a fixed IF of $f_{\mathrm{IF}} = 10\ \mathrm{MHz}$, at the same time suppressing the undesired sideband. The output of the SSB modulator is bandpass filtered to remove out of band noise and then demodulated by the PLL-based FM demodulator.

The PPF is implemented as a type-II PPF [17] consisting of coupled low- and high-pass RC-filter sections according to Fig. 2. It was designed for a passband, i.e., the band of frequencies over which it produces a nominal phase shift of 90° between its I- and Q-output signals, extending from 1 kHz to 3 MHz in order to allow for the use of cantilevers with resonance frequencies between approximately 10 kHz and 1.5 MHz and demodulation bandwidth as large as the corresponding resonance frequency, i.e., true single-cycle detection. The number of sections in the PPF has been selected to ensure a sufficiently large suppression of the image frequency, i.e., the undesired sideband, over the entire passband. Here, a high sideband suppression is important for two reasons: First, insufficient suppression of the undesired sideband creates a tone at two times the cantilever frequency, which can eventually produce distortion in the AFM image. Second, a low image rejection ratio (IRR), defined as the ratio of the power in the desired sideband and the power in the undesired sideband in the output of the SSB, causes noise from the undesired sideband to leak into the signal band, deteriorating the achievable SNR. While the former problem can be solved by the use of a low-pass filter subsequent to the PLL demodulator, the latter problem needs to be addressed during the design phase.

The amount of SNR deterioration introduced by the non-ideal quadrature generation of the PPF can be captured by an equivalent noise figure F_{PPF}, defined as the ratio of the SNR at the input of the PPF and the SNR at the output of the SSB modulator, assuming that all components in the SSB modulator except the PPF are ideal. Noting that a type-II PPF has negligible amplitude imbalance [17], the main source of error is the phase imbalance between the PPF's I- and Q-outputs, $\Delta\varphi_{\mathrm{err}} = 90^\circ - \Delta\varphi = 90^\circ - (\varphi_{\mathrm{I}} - \varphi_{\mathrm{Q}})$, where φ_{I} and φ_{Q} are the phase of the I- and the Q-output, respectively. It can be shown [18] that the relation between the noise figure F_{PPF}, the IRR and the phase error $\Delta\varphi_{\mathrm{err}}$ is given by

$$\frac{1}{F_{\mathrm{PPF}} - 1} = \mathrm{IRR} = \cot^2\left(\frac{\Delta\varphi_{\mathrm{err}}}{2}\right). \tag{1}$$

Equation (1) can be used to compute the minimum required IRR, $\mathrm{IRR}_{\mathrm{min}}$, and the corresponding maximum tolerable phase error $\Delta\varphi_{\mathrm{err,max}}$ required to achieve a certain noise figure. For our prototype system we decided to go for a noise figure of 0.01 dB, corresponding to an $\mathrm{IRR}_{\mathrm{min}}$ of 26.4 dB and a maximum tolerable phase error of $\Delta\varphi_{\mathrm{err,max}} = 5.5^\circ$. Here, it should be noted that in order to achieve a dynamic range between 40 to 60 dB, which is typically required in AFM applications, the distortion component at two times the cantilever resonance frequency, i.e., the image of the cantilever resonance frequency, has to be further suppressed by a low-pass filter succeeding the PLL-based FM demodulator with an attenuation between 15 and 35 dB at this frequency. Having defined a specification for the IRR, we found by numerical simulations in MATLAB that a PPF with eight stages is required to meet this specification over the entire PPF passband. Here, a PPF with eight stages presents a good compromise between improving IRR (requiring a large number of stages) and lowering the loss and noise introduced by the PPF.

The simulated IRR and phase error together with the corresponding measured data obtained with the PCB-based prototype described in Section IV, are plotted in Fig. 3. From the figure,

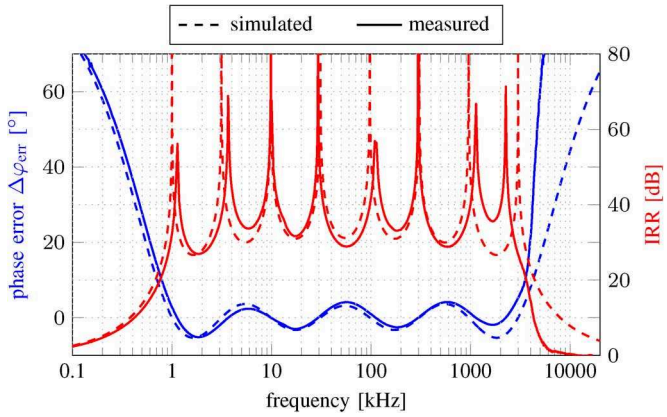

Fig. 3. Simulated and measured phase error $\Delta\varphi_{\rm err}$ and IRR of the employed eight stage type-II PPF.

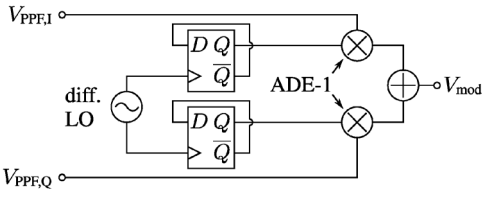

Fig. 4. LO IQ-generation and custom made IQ modulator.

we see that for low frequencies, there is a good matching between simulated and measured data. For higher frequencies, the pole and zero locations are slightly shifted from their simulated positions due to the discretization and tolerances of standard off-the-shelf passive components.

At this point, it should be noted that, although an improved IRR versus frequency behavior for a given number of filter sections could theoretically be achieved by a non-uniform placement of the PPF pole and zero frequencies [17], this improvement is typically marginal (e.g. a 1.5 dB improvement for a four-section PPF [17]) and further diminished by the component tolerances of the discrete capacitors. Consequently, in the prototype of Section IV we uniformly (on a logarithmic scale) distributed the pole and zero frequencies between 1 kHz and 3 MHz.

Due to the lack of commercially available SSB modulator chips in the frequency range of interest, the SSB modulator in the prototype of Section IV is custom-made by means of two frequency mixers (ADE-1, Minicircuits, USA) whose quadrature local oscillator (LO) signals are generated using a frequency-divide-by-two-stage consisting of two D-flip-flops according to Fig. 4. The differential LO signal feeding the flip-flops at a frequency of $f_{\rm LO} = 2(f_{\rm IF} + f_{\rm cant})$, where $f_{\rm cant}$ is the resonance frequency of the cantilever, i.e., the center frequency of the AFM signal, is generated by an external differential clock generator (CG635, Stanford Research Systems, Sunnyvale, CA, USA). According to Fig. 4, the SSB upconversion itself is then performed by adding (subtracting) the outputs of the I- and Q-mixers in order to select the lower sideband (LSB) or upper sideband (USB), respectively.

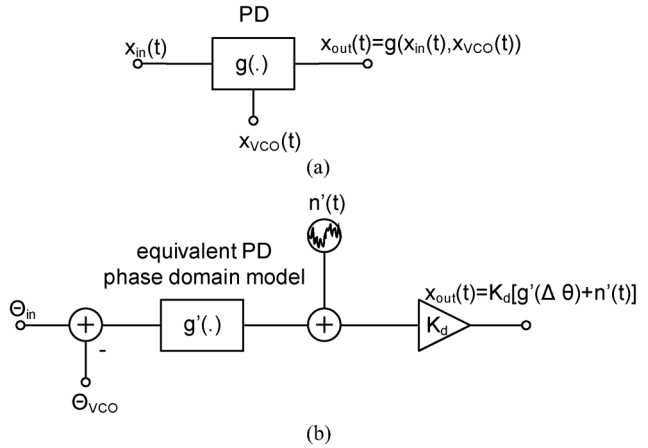

Fig. 5. Illustration of PD models (a) with noisy inputs and (b) equivalent PD phase domain model which transforms the noise at the PD input into an equivalent phase noise process $n'(t)$ at the PD output.

In order to limit the amount of integrated AM noise at the input of the PLL, the output of the quadrature modulator is filtered by a passive third order bandpass filter centered around $f_{\rm IF}$ before it is fed into the PLL-based FM demodulator. Finally, the demodulated signal is amplified and low-pass filtered by a filter stage with adjustable gain and bandwidth settings.

III. PLL Noise Model

An ideal FM demodulator is insensitive to AM noise present in its input signal. However, any real FM demodulator converts a fraction of the amplitude noise at its input into frequency noise, cf. e.g. [19] and [20], and, therefore, care has to be taken in the design process that the additional electronics of the SSB modulator, which can significantly increase the amplitude noise level at the PLL input, does not degrade the overall system noise figure. Since in a PLL-based FM demodulator the AM-to-FM noise conversion takes place in the phase detector, in this section, we will present an analytical model which predicts the contribution of the various noise sources inside the PLL-based demodulator to the PLL's input referred frequency noise including the contribution from amplitude noise at the PD input. Our analysis extends the approach presented in [19] to the special case of PLLs incorporating a phase frequency detector (PFD) because this is the PD utilized in the prototype design of Section IV. The method of [19] accounts for the nonlinear loop behavior by transforming the nonlinear PD into a transformed linearized model, cf. Fig. 5, which can then be incorporated into a standard linearized phase domain model of a PLL according to Fig. 6. Naturally, such a linearized model is only valid in the locked state of the PLL and cannot be used to analyze the PLL's large signal behavior which occurs e.g. during the lock-in process.

Following the approach of [19] we can assume that the PD input signals $x_{\rm in}(t)$ and $x_{\rm VCO}(t)$ can be modeled as a modulated signal corrupted by additive noise $n(t)$ and an ideal sine wave according to

$$\begin{aligned} x_{\rm in}(t) &= A_{\rm in}\sin(\omega_0 t + \theta_{\rm in}) + n(t) \\ &= \tilde{A}_{\rm in}(t)\sin\left(\omega_0 t + \theta_{\rm in} + \theta_{\rm n}(t)\right) \end{aligned} \tag{2a}$$

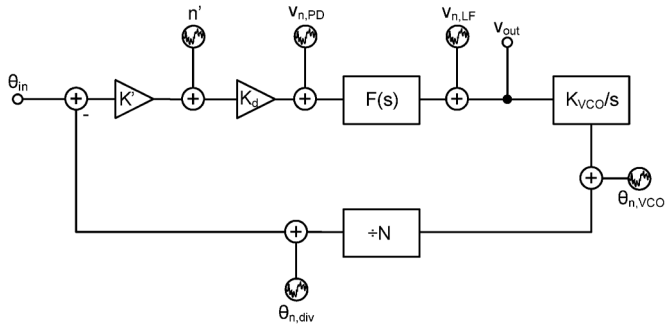

Fig. 6. PLL model incorporating the linearized PD model of Fig. 5(b) and additive noise sources for all remaining noise contributors.

$$x_{\mathrm{VCO}}(t) = A_{\mathrm{VCO}} \cos(\omega_0 t + \theta_{\mathrm{VCO}}). \tag{2b}$$

The nonlinear phase transfer characteristic $g(\Delta\theta)$ of the PD, can be replaced by a subtractor, a subsequent transformed nonlinearity $g'(\Delta\theta)$, a transformed additive noise process $n'(t)$ and the gain K_{d} of the PD according to Fig. 5(b). In (2), $\tilde{A}_{\mathrm{in}}(t)$ and $\theta_{\mathrm{n}}(t)$ are the so-called amplitude and phase noise process, respectively, and $\Delta\theta = \theta_{\mathrm{in}} - \theta_{\mathrm{VCO}}$ is the phase difference of the PD's reference and VCO input in the absence of noise. For PD input signals given by (2a) and (2b), the phase difference in the presence of noise becomes $\Delta\theta + \theta_{\mathrm{n}}(t)$ and we obtain for the signal at the PD output

$$x_{\mathrm{out}}\left(t, \Delta\theta, \theta_{\mathrm{n}}(t)\right) = K_{\mathrm{d}} \cdot g\left(\Delta\theta + \theta_{\mathrm{n}}(t)\right). \tag{3}$$

Then, assuming that the PLL's closed loop bandwidth B_{L} is much smaller than the input noise bandwidth B_{n}, the phase error $\Delta\theta$ varies much slower than the input phase noise $\theta_{\mathrm{n}}(t)$ and we can find an expression for the output of the PD in the transformed system by finding the conditional expected value of the PD characteristic given a certain (slowly time-varying) phase error $\Delta\theta$. The residual error is attributed to the zero-mean transformed noise process $n'(t)$, that is

$$\begin{aligned} x_{\mathrm{out}}(t, \Delta\theta, \theta_{\mathrm{n}}(t)) &= K_{\mathrm{d}}\left[E\left\{g\left(\Delta\theta + \theta_{\mathrm{n}}(t)\right)|\Delta\theta\right\} + n'(t, \Delta\theta)\right] \\ &= K_{\mathrm{d}}\left[g'(\Delta\theta) + n'(t, \Delta\theta)\right] \end{aligned} \tag{4}$$

where

$$g'(\Delta\theta) = E\left\{g\left(\Delta\theta + \theta_{\mathrm{n}}(t)\right)|\Delta\theta\right\}. \tag{5}$$

Then, the transformed noise process $n'(t)$ can be obtained by comparing (3) and (4) according to

$$n'(t, \Delta\theta) = g\left(\Delta\theta + \theta_{\mathrm{n}}(t)\right) - g'(\Delta\theta). \tag{6}$$

Next, we will proceed by calculating the total power $\sigma_{\mathrm{n}}'^2(\Delta\theta)$ as well as the equivalent noise bandwidth B_{n}' of the equivalent noise process $n'(t)$. Knowing $\sigma_{\mathrm{n}}'^2(\Delta\theta)$ and B_{n}', we can obtain an equivalent white power spectral density capturing the essential properties of $n'(t)$.

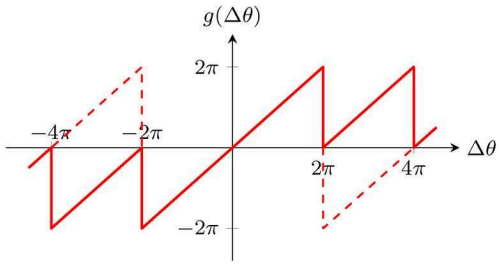

Fig. 7. Transfer characteristic of an ideal PFD (solid) and the approximation used in our calculations (dashed).

In [21] it was found that $\sigma_{\mathrm{n}}'^2(\Delta\theta)$ is a very weak function of $\Delta\theta$ and it does not deviate significantly from its maximum value at $\Delta\theta = 0$. Making use of this finding, evaluating (6) at $\Delta\theta = 0$ and utilizing the fact that $g'(\Delta\theta = 0) = 0$, we can obtain an approximate expression for $n'(t)$ independent of $\Delta\theta$ according to

$$n'(t) \approx g\left(\theta_{\mathrm{n}}(t)\right). \tag{7}$$

Evaluating the general defining (5) and (7), we can determine the transformed transfer characteristic $g'(.)$ and the statistics of $n'(t)$ for the PFD employed in the prototype of Section IV. The nonlinear phase transfer characteristic of a PFD, $g(\Delta\theta)$, is plotted as the solid curve in Fig. 7. In the figure we see that in contrast to pure phase detectors, which possess a periodic phase transfer characteristic, a PFD serves as a linear phase detector for phase differences between -2π and 2π but for phase errors with $|\Delta\theta| > 2\pi$ the phase transfer characteristic is not a periodic extension of the behavior around $\Delta\theta = 0$. This feature of the PFD phase transfer characteristic enables the PFD to detect frequency differences and react to them more efficiently than a simple phase detector. Unfortunately, the approaches of [19] and [20] rely on a periodic phase transfer characteristic $g(\Delta\theta)$ because they make use of a Fourier expansion of $g(\Delta\theta)$. This problem can be solved by noting that in the locked state, i.e., once the PLL has acquired the frequency of the input signal, the phase error will be confined to the interval $[-2\pi, 2\pi]$, even in the presence of moderate noise. Then, the error introduced by using a 4π periodic extension of the linear PFD phase characteristic between $[-2\pi, 2\pi]$, indicated by the dotted line in Fig. 7, will be small and we can use the Fourier series based approach suggested in [19] and [20] to compute $g'(.)$ and the statistics of $n'(t)$. The Fourier series corresponding to the dotted line in Fig. 7 is given by

$$g(\Delta\theta) = 4\sum_{k=1}^{\infty} \frac{(-1)^{k+1}}{k} \sin\left(\frac{k}{2}\Delta\theta\right). \tag{8}$$

Inserting (8) into (5) and simplifying the expression using the addition theorem $\sin(x+y) = \sin x \cos y + \cos x \sin y$ in com-

bination with the even symmetry of the probability density function (pdf) of θ_{n} yields

$$g'(\Delta\theta) = 4\sum_{k=1}^{\infty}\frac{(-1)^{k+1}}{k}E\left\{\sin\left(\frac{k}{2}(\Delta\theta+\theta_{\mathrm{n}})\right)|\Delta\theta\right\} = 4\sum_{k=1}^{\infty}\frac{(-1)^{k+1}}{k}E\left\{\cos\left(\frac{k}{2}\theta_{\mathrm{n}}\right)\right\}\sin\left(\frac{k}{2}\Delta\theta\right). \quad (9)$$

Here, $E\{\cos((k/2)\theta_{\mathrm{n}})\} = \mu_k$ is the so-called signal suppression factor which can be calculated from the pdf of θ_{n}, $p(\theta_{\mathrm{n}})$, according to

$$\mu_k = E\left\{\cos\left(\frac{k}{2}\theta_{\mathrm{n}}\right)\right\} = \int_{-2\pi}^{2\pi}\cos\left(\frac{k}{2}\theta_{\mathrm{n}}\right)p(\theta_{\mathrm{n}})\mathrm{d}\theta_{\mathrm{n}}. \quad (10)$$

The pdf $p(\theta_{\mathrm{n}})$ can be calculated using the method suggested in [22] and is given by

$$p(\theta_{\mathrm{n}}) = \frac{1}{4\pi\sigma_{\mathrm{n}}^2}\int_0^{\infty}A\cdot\exp\left\{-\frac{A^2+A_{\mathrm{in}}^2-2A_{\mathrm{in}}A\cos\frac{\theta_{\mathrm{n}}}{2}}{2\sigma_{\mathrm{n}}^2}\right\}\mathrm{d}A \quad (11)$$

with $-2\pi < \theta_{\mathrm{n}} < 2\pi$ and $0 < A < \infty$. Then, inserting (11) into (10) and following the approach outlined in [20] we can compute an analytical expression for μ_k according to

$$\mu_k = \sqrt{\pi\mathrm{CNR}}\exp\left\{-\frac{\mathrm{CNR}}{2}\right\}\left[I_{\frac{k-1}{2}}\left(\frac{\mathrm{CNR}}{2}\right)+I_{\frac{k+1}{2}}\left(\frac{\mathrm{CNR}}{2}\right)\right] \quad (12)$$

where $I_k(.)$ is the modified Bessel function of order k and CNR is the input carrier to noise ratio given by

$$\mathrm{CNR} = \frac{A_{\mathrm{in}}^2}{2\sigma_{\mathrm{n}}^2} \quad (13)$$

where σ_{n}^2 is the variance of the additive input amplitude noise process.

According to the discussion above, in order to obtain an approximate expression for the power spectral density (PSD) of the transformed noise process $n'(t)$, we will replace it by a white noise process with variance σ'_{n} and bandwidth B'_{n}. This assumption can be justified by the previously stated observation that the equivalent noise bandwidth of the original additive input noise process, B_{n}, is much larger than the closed loop PLL bandwidth. Additionally, as we shall see momentarily, the resulting equivalent noise bandwidth of the transformed noise process, B'_{n}, only marginally deviates from B_{n}, indicating that $n'(t)$ is approximately white.

Following this reasoning, the PSD of $n'(t)$ is approximately given by

$$S_{N'N'} = \frac{\sigma_{\mathrm{n}}'^2}{B'_{\mathrm{n}}}. \quad (14)$$

The variance $\sigma_{\mathrm{n}}'^2$ can be calculated using (7) and the pdf of θ_{n}, $p(\theta_{\mathrm{n}})$, according to

$$\sigma_{\mathrm{n}}'^2 = \int_{-2\pi}^{2\pi}g^2(\theta_{\mathrm{n}})p(\theta_{\mathrm{n}})\mathrm{d}\theta_{\mathrm{n}}. \quad (15)$$

Following the approach outlined in [19] to solve (15) yields

$$\sigma_{\mathrm{n}}'^2 = 4\cdot\left(\frac{\pi^2}{3}+4\sum_{k=1}^{\infty}(-1)^k\frac{\mu_k}{k^2}\right). \quad (16)$$

As discussed in [19], the nonlinearity of the PD does not significantly affect the equivalent noise bandwidth and the error introduced by approximating it with the equivalent noise bandwidth of a sawtooth PD according to

$$B'_{\mathrm{n}} = B_{\mathrm{n}}\left(1+0.35\cdot\exp\left\{-\mathrm{CNR}\left(1-\frac{\pi}{4}\right)\right\}\right) \quad (17)$$

is small. At this point, it is instructive to look at the two limiting cases of the equivalent noise bandwidth for small and large CNR's, i.e.

$$B'_{\mathrm{n}} = B_{\mathrm{n}}, \quad \mathrm{CNR}\gg 1 \quad (18a)$$
$$B'_{\mathrm{n}} = 1.35\cdot B_{\mathrm{n}}, \quad \mathrm{CNR}\ll 1. \quad (18b)$$

The equivalent phase detector model of Fig. 5(b) can be incorporated into the standard phase domain PLL model of Fig. 6 where all noisy components are replaced by additive equivalent noise sources, cf. e.g. [16] and [23]. Assuming moderate fluctuations due to noise, the nonlinear PD transfer characteristic can be linearized around its operating point using the equivalent gain K'_{d}, cf. [19] or [23]. For the PFD employed in our prototype design K'_{d} is given by

$$K'_{\mathrm{d}} = \left.\frac{\mathrm{d}g'(\Delta\theta)}{\mathrm{d}\Delta\theta}\right|_{\Delta\theta=0} = 4\sum_{\nu=1}^{\infty}(-1)^{\nu+1}\mu_\nu. \quad (19)$$

Using this model, we have performed numerical simulations in MATLAB to compute the contribution of each noise source of Fig. 6 to the PLL's input referred frequency noise. For our simulations we have chosen the loop filter topology shown in Fig. 8, i.e., an active 3rd order low-pass filter, which is also implemented in the PCB-based prototype of Section IV. In this filter topology the classic $RC-C$ loop filter structure which transforms the charge pump current into a voltage is augmented by an active section, which allows for the use of an external

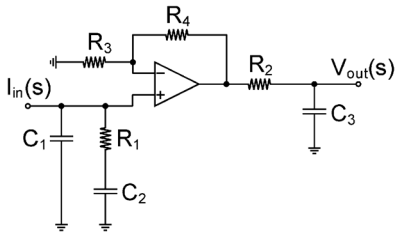

Fig. 8. Schematic of the utilized loop filter topology. Capacitors C_1 and C_2 and resistor R_1 transform the current from the PFD charge pump combination into a voltage and the remaining circuitry provides a further pole which can incorporate the large load capacitance of the discrete VCO.

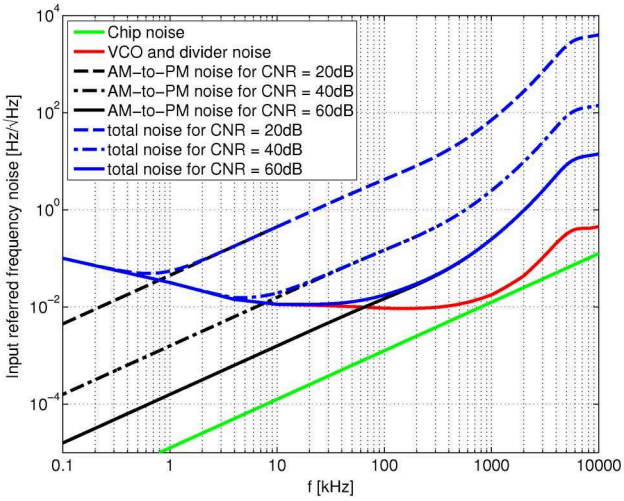

Fig. 9. Simulation results for the input referred frequency noise of the PLL-based FM demodulator for three different levels of AM noise at the PLL input. The remaining simulation parameters correspond to the PCB based prototype described in Section IV and are given by: $C_1 = 11\,\mathrm{pF}$, $C_2 = 876\,\mathrm{pF}$, $C_3 = 1.233\,\mathrm{nF}$, $R_1 = 1.47\,\mathrm{k\Omega}$, $R_2 = 12\,\Omega$, $R_3 = 1\,\mathrm{k\Omega}$, $R_4 = 220\,\Omega$, VCO: Minicircuits ROS-70-119+, PLL chip: Analog Devices ADF4002, charge pump current $I_{\mathrm{CP}} = 5\,\mathrm{mA}$.

VCO with its large parasitic input capacitance. The loop filter's transfer function $F(s)$ is given by

$$K_{\mathrm{d}}F(s) = \frac{I_{\mathrm{CP}}}{2\pi}\frac{b-1}{b}\frac{R_3}{R_3+R_4}\frac{1+s\tau_1}{\left(1+\frac{s\tau_1}{b}\right)sC_1}\frac{1}{1+s\tau_{\mathrm{out}}} \tag{20}$$

where I_{CP} is the charge pump current, $b = 1 + C_1/C_2$, $\tau_1 = R_1C_1$ and $\tau_{\mathrm{out}} = R_2C_3$. The loop filter is designed for a closed-loop bandwidth of 1 MHz and a phase margin of 70° using the software tool ADIsimPLL (Analog Devices, Norwood, MA, USA). Simulation results of the input referred frequency noise spectral density for three different input carrier to noise ratios are shown in Fig. 9. The model parameters used for the simulation are listed in the figure caption. In the figure, we see that for low frequencies the input referred frequency noise is dominated by the VCO and divider noise and that a corner frequency exists at which the transformed amplitude noise becomes the dominant noise source. For frequencies larger than this corner frequency, the total input referred frequency noise increases with a slope of 20 dB/dec.

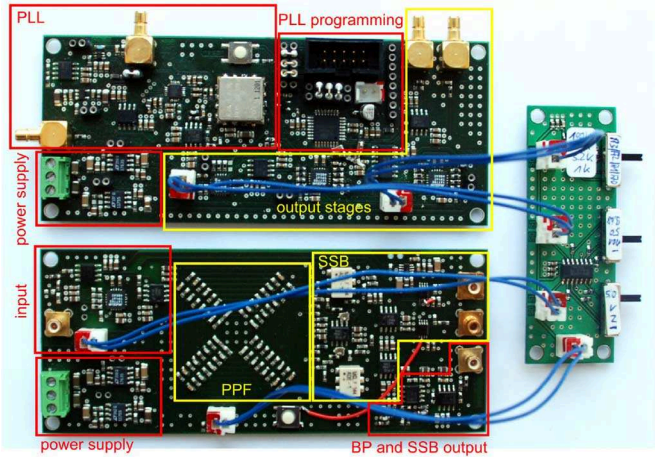

Fig. 10. Annotated picture of the fabricated PCB-based FM demodulator prototype.

IV. PCB-Based Prototype

In order to validate the proposed demodulator architecture experimentally, we have designed and fabricated a PCB-based prototype with discrete off-the-shelf electronics. Annotated photographs of the prototype PCBs are shown in Fig. 10. In the figure, the bottom PCB implements the SSB upconversion and the top one realizes the PLL-based FM demodulation.

In order to render the electronics compatible with commercially available AFMs, the prototype design incorporates an input stage with programmable gain settings which can be used to adjust the signal levels coming from the position sensitive detector to the levels required by the on-board signal processing electronics. In the current implementation, the PLL-based FM demodulator (PLL-chip: ADF4002, Analog Devices, feedback divider setting $N = 7$, VCO: ROS-70-119+, Minicircuits, VCO quiescent frequency $f_{\mathrm{VCO}} = 70\,\mathrm{MHz}$) is designed for a demodulation bandwidth of 1 MHz. The demodulator is followed by tunable low-pass filter stages with variable gain and bandwidth settings (gain settings: 9.7, 50, 101, corner frequencies of the 4th order Butterworth filters: 1 kHz, 3.2 kHz, 10 kHz and 100 kHz) which allow the demodulator to be adjusted for different cantilever resonance frequencies and scan rates. The maximum cutoff frequency of 100 kHz was selected because according to the simulation results of Section III, for CNR values between 20 and 40 dB as they frequently occur in AFM experiments, this is approximately the maximum bandwidth for which the SNR of the demodulated signal is not deteriorated by the additional noise introduced by the SSB upconverter. The different settings can be selected by three switches mounted on a separate PCB. In addition to the signal processing electronics, the PCBs also contain the electronics for a stable and low-noise supply voltage generation and a microcontroller to program the ADF4002 through its SPI interface at power-up.

V. Measurements

In this section, we will present and discuss measured data obtained using the prototype presented in the previous section.

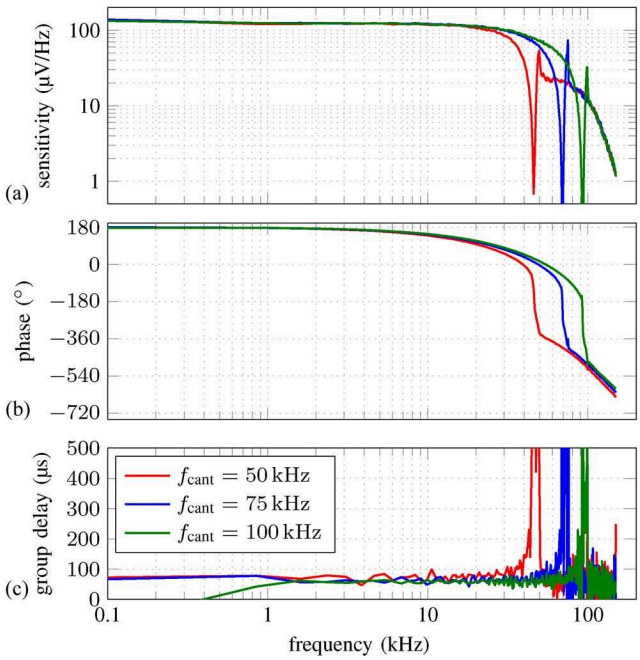

Fig. 11. Measured frequency response for cantilever resonance frequencies of 50 kHz, 75 kHz and 100 kHz. (a) Demodulation sensitivity, (b) output phase, and (c) group delay for an output gain setting of 101 and a low-pass corner frequency of 100 kHz as a function of modulation frequency. The roll-off in the phase response is mostly caused by the signal generator used to synthesize the FM modulated input signals.

The first part of this discussion will be dealing with the electrical characterization of the prototype including its input referred noise and demodulation bandwidth while in the second part, we will present preliminary AFM data.

A. *Electrical Characterization*

The key specifications for an FM-demodulator for AFM applications are its demodulation sensitivity, i.e., the change in voltage at the FM-demodulator output for a given frequency change at the PLL input, its demodulation bandwidth, its input referred noise and its limit of detection (LOD).

To measure the low-frequency demodulation sensitivity, we used a signal generator with FM generation capabilities (SG386, Stanford Research Systems, Sunnyvale, CA, USA) as input signal to the SSB modulator and recorded the output using an oscilloscope. In this way we obtained low-frequency demodulation sensitivities of 12 V/Hz, 64 V/Hz and 129 V/Hz for the three different gain settings in the filter section succeeding the PLL demodulation output.

To measure the demodulation sensitivity as a function of modulation frequency, we used the external modulation input of the SG386. Feeding this input with the output of a network analyzer (Agilent 4395A, Agilent Technologies, Santa Clara, CA, USA) and connecting the demodulated signal at the PLL output to the network analyzer's input, we recorded the demodulation frequency responses of Fig. 11 for the three different input carrier frequencies of 50 kHz, 75 kHz and 100 kHz. In all these measurements, the gain and the corner frequency of the low-pass filter succeeding the PLL were set to 101 and 100 kHz, respectively. According to Fig. 11(a), the system displays a flat demodulation response up to about 65% of the resonance frequency followed by a sharp roll-off. More specifically, for the three different input carrier frequencies of 50 kHz, 75 kHz and 100 kHz we measured 3 dB-cutoff frequencies of 36 kHz, 49 kHz and 56 kHz, respectively. These cutoff frequencies correspond to usable modulation rates normalized to the carrier of 72%, 65% and 56%. Here, the decreased value of 56% for a center frequency of $f_{\text{cant}} = 100\,\text{kHz}$ is caused by the corner frequency of the output low-pass filter at 100 kHz. The phase response of the SSB-upconverter demodulator combination as a function of the input modulation frequency is plotted in Fig. 11(b) for the same three different input carrier frequencies of 50 kHz, 75 kHz and 100 kHz, respectively. The corresponding group delay is shown in Fig. 11(c). The group delay remains at around 70 s for frequencies up to 65% of the respective cantilever resonance frequency. At this point it should be noted that for frequencies beyond approximately 10% of the carrier frequency, the signal generator itself introduces a significant frequency dependent phase shift and the measured phase responses present worst case estimates of the actual demodulation performance.

Having obtained the demodulation sensitivity as a function of modulation rate, we proceeded by measuring the FM-demodulators input referred frequency noise for three different input carrier frequencies ($f_{\text{cant}} = 50\,\text{kHz}$, 100 kHz and 300 kHz). To this end, we recorded the PLL's output noise spectrum using a spectrum analyzer (Agilent 4395A, Agilent Technologies, Santa Clara, CA, USA) and referred the noise back to the PLL's input by dividing it by the demodulation sensitivity. During these measurements the PLL was set to its highest sensitivity setting. The low pass filter at the output of the PLL was bypassed in order to experimentally verify the increase in input referred frequency noise due to the AM-FM conversion for higher frequencies discussed in Section III. The larger carrier frequency of 300 kHz was also selected to highlight the large range of cantilever resonance frequencies the proposed prototype can deal with.

The input referred frequency noise spectra measured for the three different center frequencies are shown in Fig. 12. From the figure we see that the noise is a very weak function of the input center frequencies but there are spurious tones in the spectrum at multiples of the input center frequency f_{cant}. These spurious tones originate in the LO leakage of the SSB modulator, which is measured at −45 dBc in the current prototype. Additionally, one clearly sees the effect of the PLL bandwidth of 1 MHz in the measured spectra limiting the high frequency noise. Overall, the measured frequency noise spectrum matches well (better than a factor of 2) with the model presented in Section III. According to the discussion there, for lower frequencies, the noise spectrum is dominated by the VCO and divider noise and the converted amplitude noise starts to dominate at a corner frequency around 50 kHz.

From the measured spectra of Fig. 12, we also determined the integrated frequency noise and the corresponding limit of detection of the presented FM-demodulator. The measured integrated frequency noise over a bandwidth of 50 kHz is 4.6 Hz_{rms}.

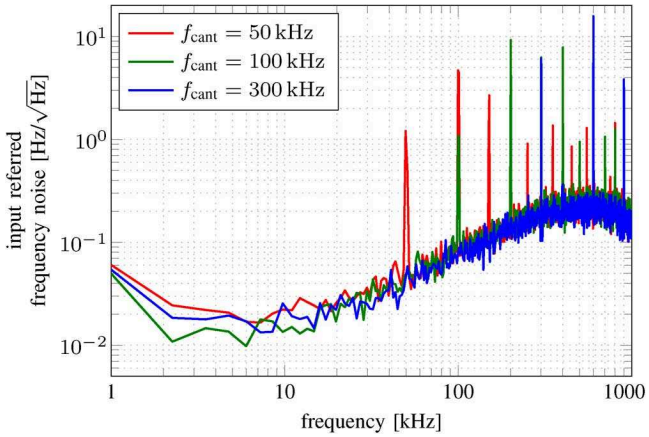

Fig. 12. Measured input referred frequency noise floor of the PCB-based prototype for input center frequencies of 50 kHz, 100 kHz, and 300 kHz, respectively.

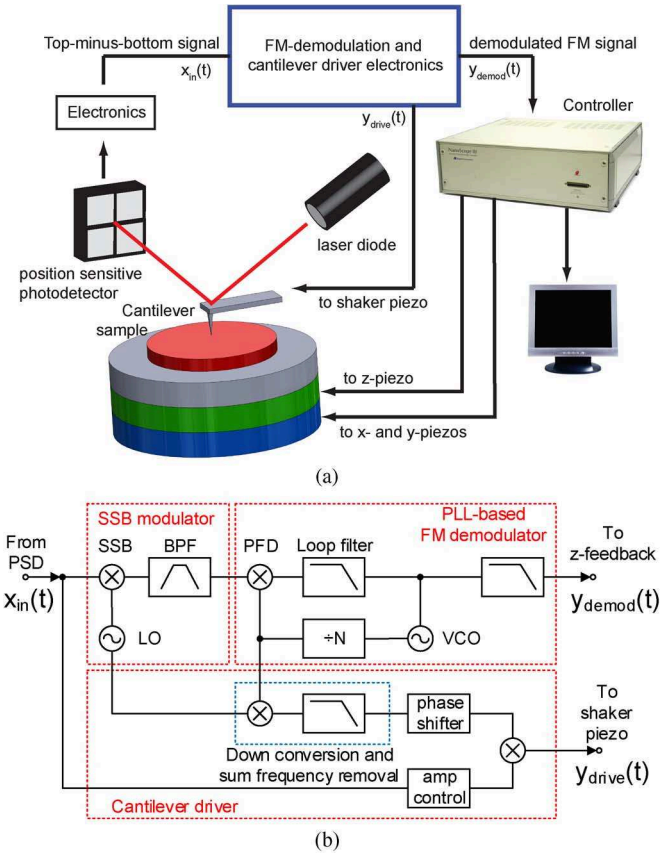

Fig. 13. (a) Illustration of the setup used to perform preliminary FM-AFM experiments using the proposed FM-demodulator architecture. (b) Detailed view of the architecture of the blue box in (a).

Defining the limit of detection, i.e., the minimum detectable frequency shift at the PLL input, as three times the integrated rms noise, we obtain an LOD of 14 Hz.

B. AFM-Imaging

In order to test the proposed demodulator architecture in the target AFM application, we performed preliminary FM-AFM experiments using the setup shown in Fig. 13. Here, Fig. 13(a) shows the overall setup including the AFM controller in order to illustrates the location of the inputs and outputs of our custom made driving/demodulation electronics, indicated by the blue box inside the figure, in the overall AFM setup. Fig. 13(b) then provides a more detailed view of the architecture of the custom-made driving and demodulation electronics.

According to Fig. 13(b), the signal coming from the position sensitive detector's top-minus-bottom signal is fed to both the SSB modulator and custom-designed AFM driver electronics similar to the one described in [24, chapter 2]. In the driver electronics, the block labeled "amp control" first extracts the current amplitude of the cantilever oscillation by means of a full-wave rectifier. The extracted amplitude is then compared against an adjustable setpoint. The resulting error signal is amplified and then used as the new amplitude value which is sent to the shaker piezo. A normalized amplitude signal at the oscillation frequency is extracted from the PLL's VCO-divider output. Since the PLL operates around 10 MHz the signal from the PLL needs to be downconverted to the cantilever resonance frequency by means of the same local oscillator which is used for the SSB upconversion. The low-pass filter which removes the sum frequency at the downconversion mixer output is followed by an adjustable phase shifter which is used to adjust the overall phase in the feedback loop to be zero at the cantilever resonance frequency, ensuring that the cantilever oscillation takes place at this frequency. The demodulated FM-signal at the PLL output is fed back as the error signal to a standard AFM controller for AM-AFM (Nanoscope V inside a Bruker Multimode 8, Bruker, Santa Barbara, CA, USA) instead of the deflection signal used in AM-AFM. The AFM controller then produces the feedback signal driving the z-piezo actuator to control the frequency shift.

Fig. 14 shows an FM-AFM image of a Mica sample obtained using the setup of Fig. 13. From left to right the figure shows (a) the height image, (b) the error image, and (c) the 3D height image of the same region on the Mica sample. The displayed topography image was processed using the software described in [25]. The image is taken at a scan rate of 1 Hz per line with an OTESPA cantilever with a resonance frequency of 278.8 kHz. The frequency sensitivity in the error image is about 5 nm/V. Although the imaging speed was limited by the standard AFM scanner and controller (Bruker Multimode 8 AFM, EV-Scanner, Bruker, Santa Barbara, CA, USA) used to perform the experiments, the image of Fig. 14 clearly serves as a proof-of-principle for the proposed modified FM-AFM setup.

VI. Conclusion and Outlook

In this paper, we have presented a new architecture for high-speed PLL-based FM demodulation for real-time AFM applications incorporating an SSB modulator. The SSB upconversion allows the PLL to operate at a higher center frequency, removing the PLL's intrinsic bandwidth limitation and thereby allowing for a true single-cycle FM detection. We have identified the AM noise added by the SSB modulator, which is converted into frequency noise in the PLL's PD, as the limiting factor for the achievable detection bandwidth of the system. The model of this AM-to-FM conversion presented in Section III allows to quantify this limitation and thus to account for it during the design phase. In Section V, we have presented measured results of

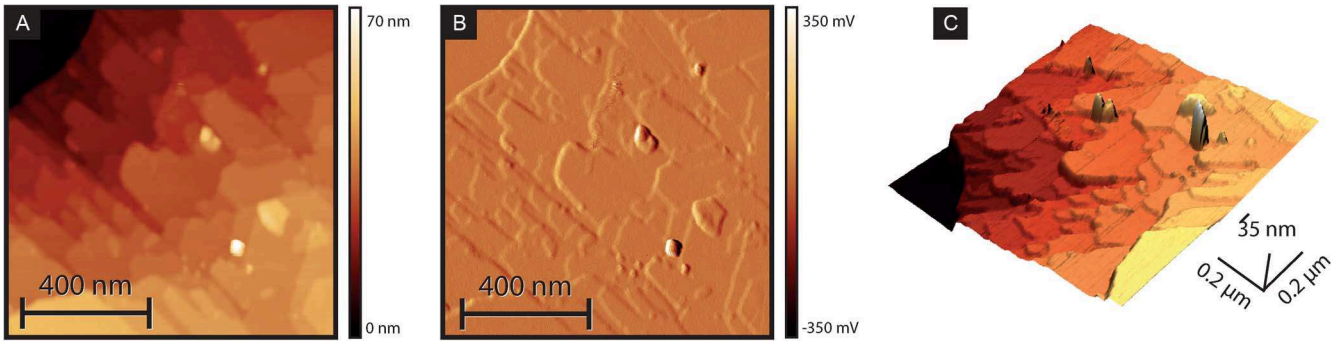

Fig. 14. (a) Height image, (b) error image and (c) 3D height image of a Mica sample obtained using the FM-AFM setup of Fig. 13.

a PCB-based prototype of the proposed system which both validates the PLL model of Section III and provides a proof-of-principle that the proposed detector architecture can indeed increase the PLL bandwidth without deteriorating the system noise figure over a certain frequency band. With its integrated frequency noise of about 4.6 $\mathrm{Hz_{rms}}$ in a frequency bandwidth of 50 kHz, the present prototype can demodulate AFM signals originating from a cantilever with a resonance frequency of 50 kHz and the corresponding maximum scan rate without SNR degradation due to the additional hardware. A larger demodulation bandwidth up to 1 MHz is possible with the existing prototype but at the cost of a degraded SNR due to the positive slope of the frequency noise floor originating from the transformed AM noise. Here, it should be noted that despite the degraded SNR due to the converted AM-noise, up to the largest bandwidth of 1 MHz, the limit of detection of the presented prototype remains better than 0.1% of the cantilever resonance frequency which is sufficient for AFM applications. To further improve the achievable frequency resolution for large demodulation bandwidths, we are currently working on an improved prototype with a lower AM noise floor which will allow to work with even higher cantilever resonance frequencies and the corresponding increased demodulation bandwidths. On a longer time-scale, we are also working on an integrated circuit (IC) implementation of the proposed demodulator architecture. The increased flexibility of an IC implementation compared to off-the-shelf components will allow us to build a custom SSB-PLL combination optimized for an intermediate frequency around 100 MHz and a corresponding PLL bandwidth up to 10 MHz. Such a system will allow for a true single-cycle detection of the FM signals produced by the fastest cantilevers available today with resonance frequencies around 5 MHz. In addition to this work on the FM-demodulator, we are also improving the driving electronics of Fig. 13 in order to fully benefit from the increased demodulation bandwidth of the proposed FM-demodulator in real-time AFM experiments conducted using the custom highspeed AFM systems developed in the Laboratory for Bio- and Nano-Instrumentation at EPFL.

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